

Counters

- Counter is a specialized **register**
- Goes through a prescribed sequence of states upon the application of input pulses
- Two categories based on different design styles:
 - **Asynchronous counter / Ripple counter**: Some FFs are triggered NOT by the common clock pulse, but by **the transition in other FF outputs**
 - **Synchronous counter**: All FFs are triggered by the **common clock pulse**

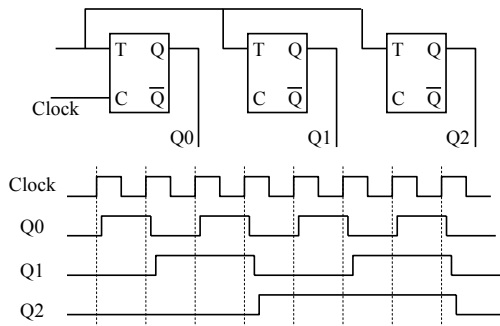
1

Overview

Category	Direction	FF Type	Additional Feature
Asynchronous	Up	T	
Asynchronous	Down	T	
Synchronous	Up	T	
Synchronous	Up	T	Enable
Synchronous	Up	D	Enable
Synchronous	Up	D	Enable / Parallel Load
Asyn / Syn	Up	T / D	Modulo-7

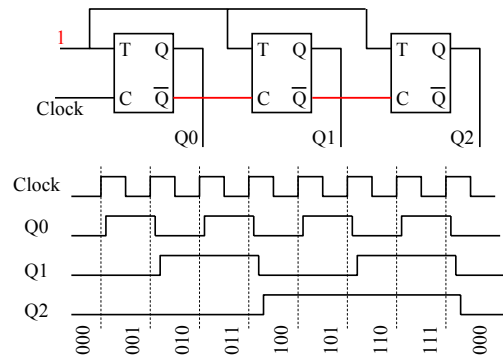
2

Asynchronous Up-Counter using T Flip-Flops



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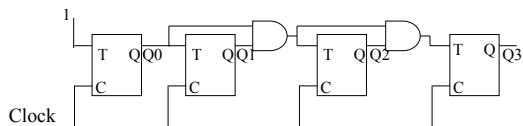
Asynchronous Up-Counter using T Flip-Flops



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Synchronous Up-Counter using T Flip-Flops

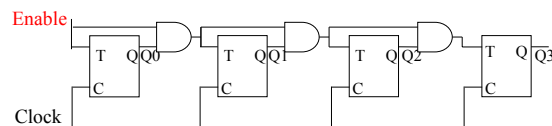
- For a 4-bit Up-Counter, the input T_i is defined as:
 - $T_0 = 1$
 - $T_1 = Q_0$
 - $T_2 = Q_0 \cdot Q_1$
 - $T_3 = Q_0 \cdot Q_1 \cdot Q_2$



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Synchronous Up-Counter with Enable using T FFs

- For a 4-bit Up-Counter with Enable, the input T_i is defined as:
 - $T_0 = \text{ENABLE}$
 - $T_1 = Q_0 \cdot \text{ENABLE}$
 - $T_2 = Q_0 \cdot Q_1 \cdot \text{ENABLE}$
 - $T_3 = Q_0 \cdot Q_1 \cdot Q_2 \cdot \text{ENABLE}$



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